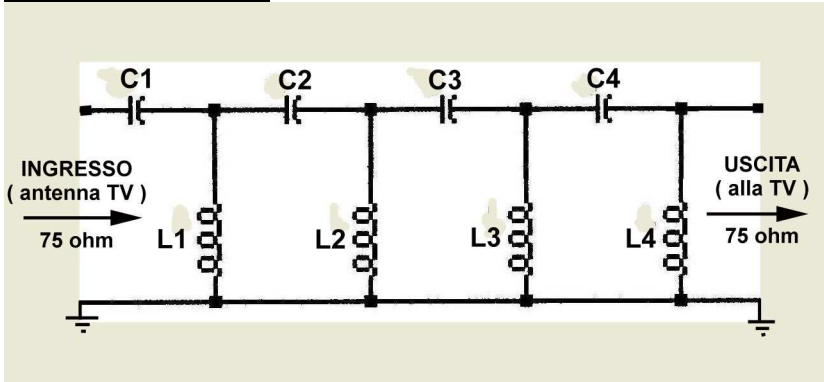


FILTRO ANTI - TVI

IW5ACP

Schema elettrico



Elenco componenti

C1 = 33 pF ceramico NPO 50 VL

C2 = 8 pF ceramico NPO 50 VL

C3 = 7 pF ceramico NPO 50 VL

C4 = 12 pF ceramico NPO 50 VL

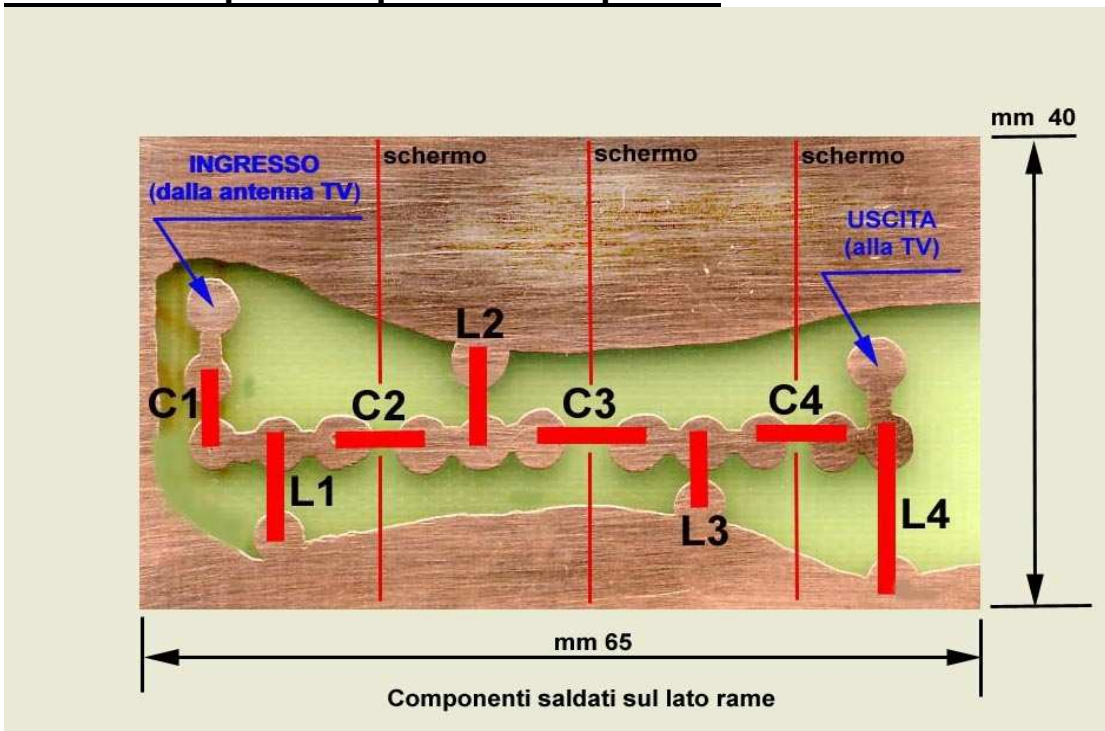
L1 = 3 spire rame argentato D=1mm su D=8 mm spaziatura fra le spire 1mm

L2 = 3 spire rame argentato D=1mm su D= 4mm spaziatura fra le spire 1mm

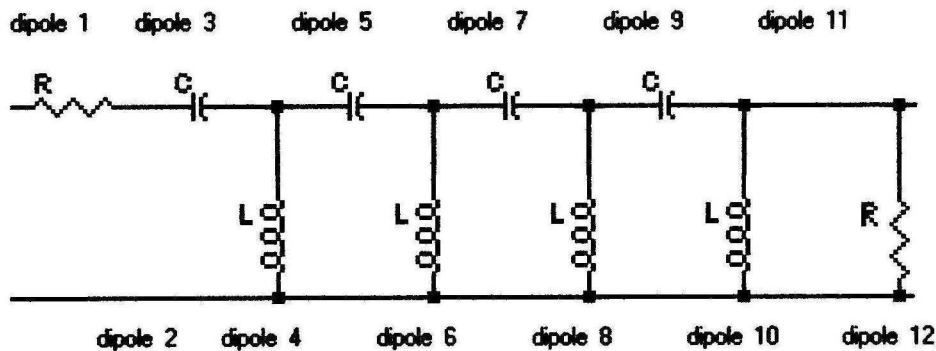
L3 = 2 spire rame argentato D=1mm su D=8mm spaziatura fra le spire 1mm

L4 = 6 spire rame argentato D=1mm su D=8mm spaziatura fra le spire 1mm

Circuito stampato e disposizione componenti



Schema elettrico per simulazione



DIPOLE 1
 R 1=75.

DIPOLE 3
 C 3=33,pF

DIPOLE 4
 L 4=65,nHy
 Qu~200,
 F(L4C3)=
 108,669203MHz

DIPOLE 5
 C 5=8,pF
 F(C5L4)=
 220,708195MHz

DIPOLE 6
 L 6=37,nHy
 Qu~200,
 F(L6C5)=
 292,532603MHz

DIPOLE 7
 C 7=7,pF
 F(C7L6)=
 312,730507MHz

DIPOLE 8
 L 8=43,nHy
 Qu~200,
 F(L8C7)=
 290,092756MHz

DIPOLE 9
 C 9=12,pF
 F(C9L8)=
 221,562002MHz

DIPOLE 10
 L 10=185,nHy
 Qu~200,
 F(L10C9)=
 106,817804MHz

DIPOLE 12
 R 12=75.

8,th order TVI
 Stopband = 4,197 db minimum @ 160,Mhz
 Cutoff = 3, db @ 165,Mhz
 Design Impedance=75, ohms
 Input Impedance = 75, ohms
 Output Impedance = 75, ohms
 Capacitance Spread = C 3 : C 7 = 4,714
 Inductance Spread = L 10 : L 6 = 5,

Grafico risposta in frequenza (teorico)

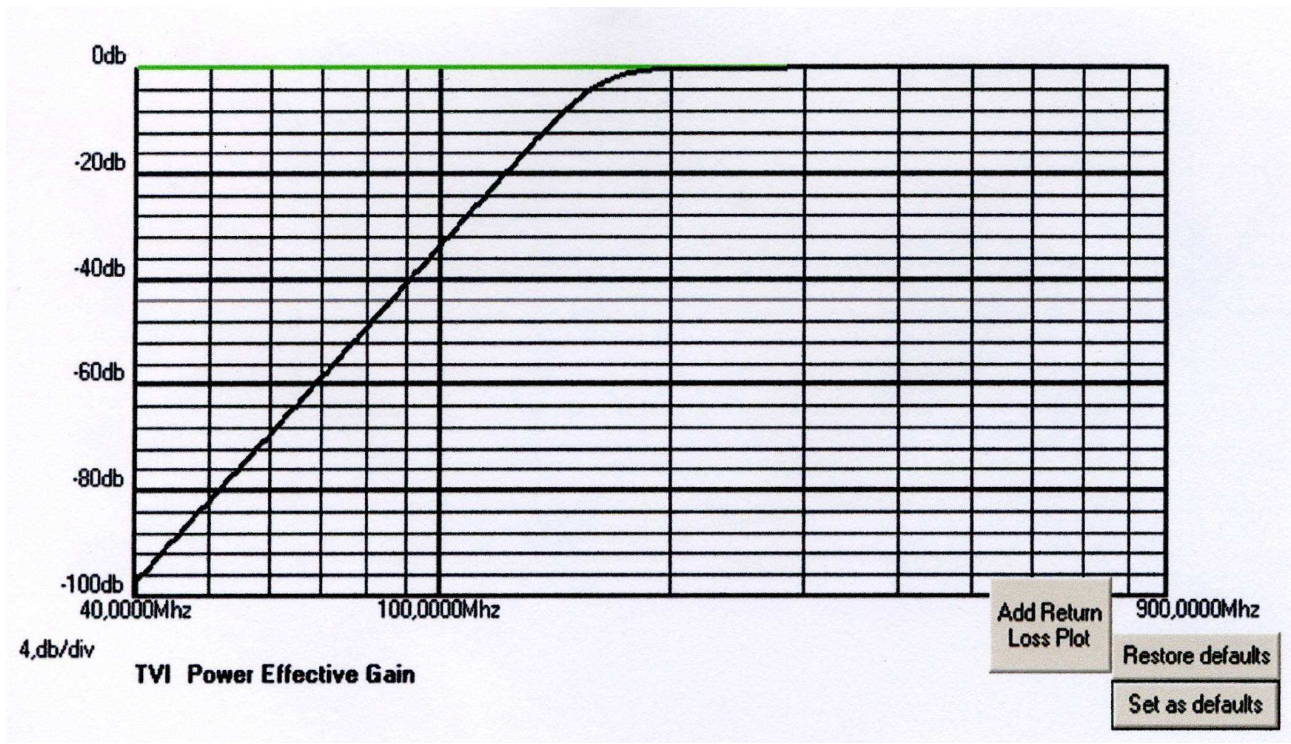


Grafico impedenza di ingresso (teorico)

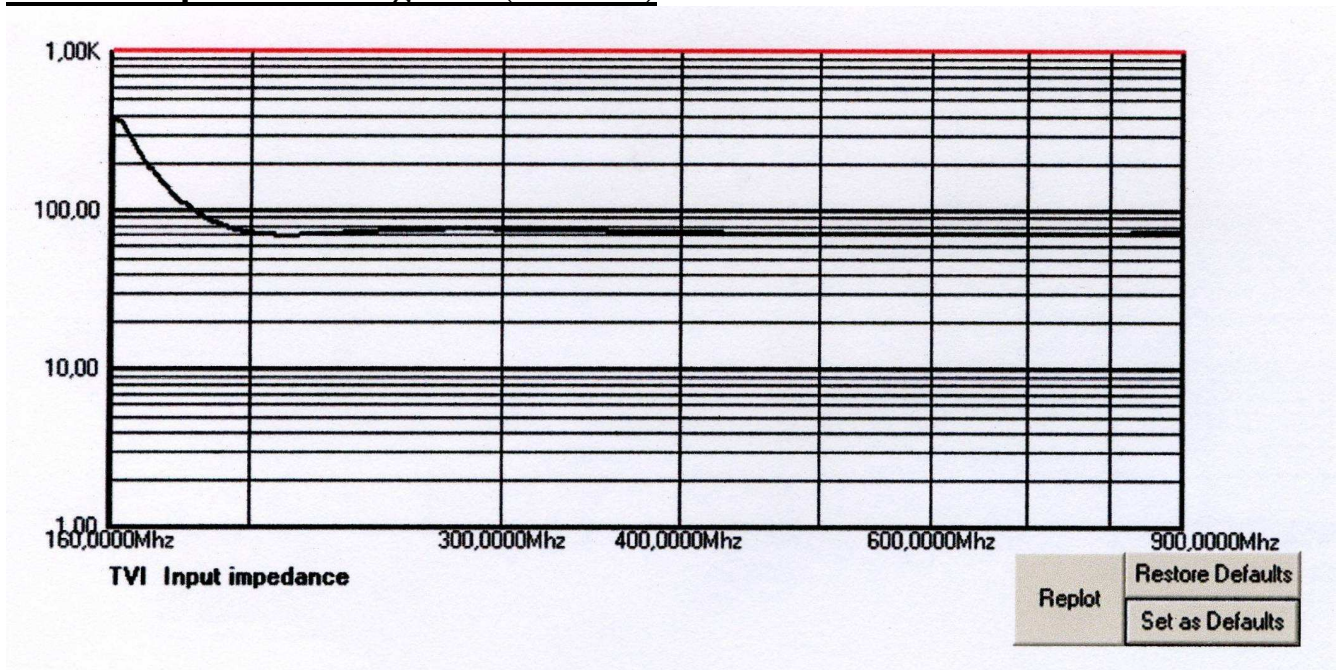


Grafico impedenza di uscita (terico)

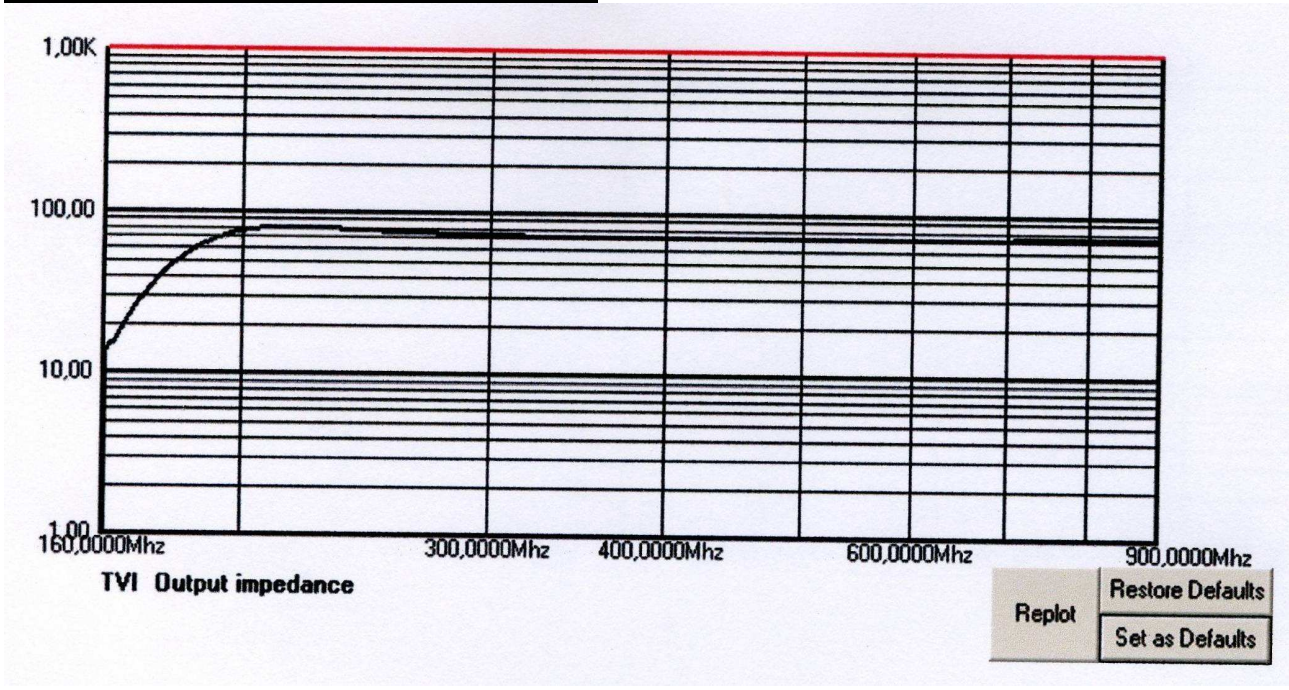
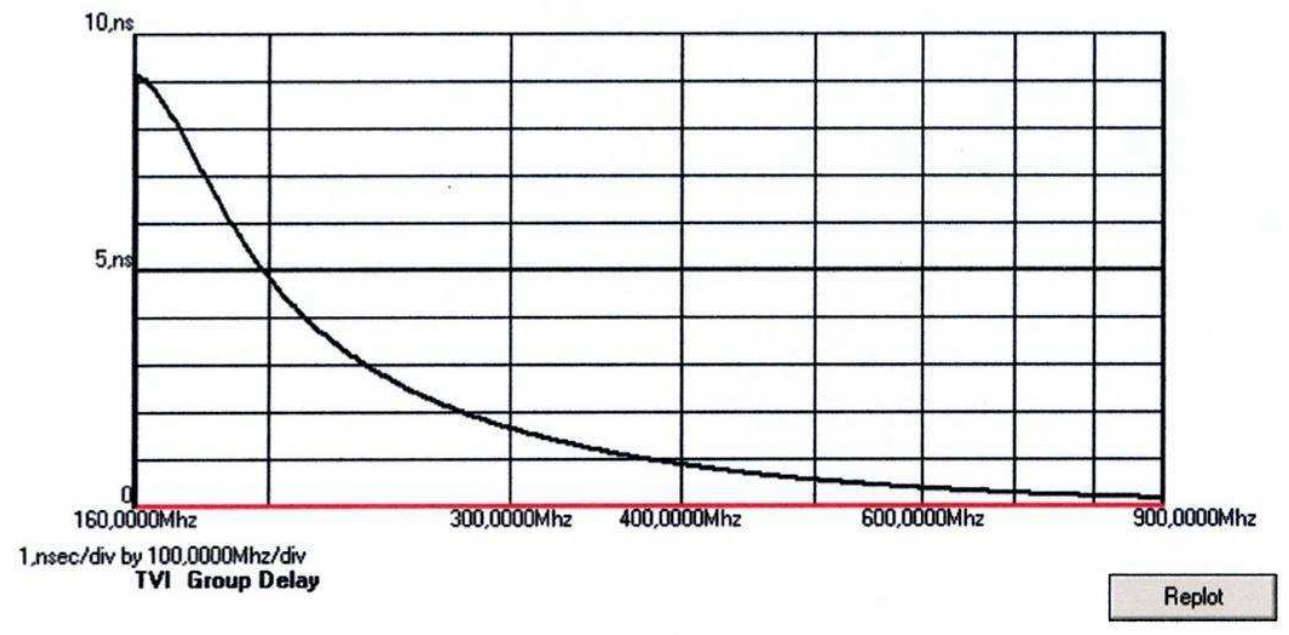


Grafico ritardo di gruppo (teorico)





**Filtro anti - TVI
IW5ACP**

**Filtro anti - TVI
IW5ACP**

**Dimensioni contenitore
base: mm 70 x 55
altezza: mm 25**



Filtro anti - TVI
IW5ACP

